Instruction Sampling in a Microprocessor

ABSTRACT

The problem identified above is addressed in large part by a microprocessor as disclosed herein. The microprocessor includes a dispatch unit configured to receive a set of instructions from an instruction cache and to forward the set of instructions to an issue queue when the instructions are ready for execution. The dispatch unit may include sampling logic that is configured to select one of the instructions for performance monitoring from the set of instructions. The microprocessor further includes a performance monitor unit enabled to monitor performance characteristics of the selected instruction as it executes. The sampling logic may identify the instruction selected for monitoring as the instruction occupying an eligible position within the set of instructions. The eligible position from which the monitored instruction is selected may vary with each subsequent set of instructions. The sampling logic may include a selection mask that contains an asserted bit that identifies the position within the set of instructions from which the selected instruction is chosen. The selection mask may include a single bit for each position in the set of instructions and may be implemented as a shift register that periodically rotates the eligible position. The rotation of the eligible bit position may occur every clock cycle, every dispatch cycle, or at some another suitable synchronous or asynchronous interval. The selection mask may contain multiple asserted bits and may include a filter circuit that generates a selection vector based on the selection mask where the selection vector includes only a single asserted bit.